Amendments to the Claims

Please amend the claims according to the following directions. Please replace all prior versions and listings of claims in this application with the following list of claims:

1. (previously amended) A method for synchronizing parallel texture pipelines, comprising:

loading an array of state variables for a polygon into an accumulation portion of a plurality of parallel texture pipelines; and then

simultaneously enabling a processing portion of a number of the parallel texture pipelines, said number corresponding to a number of parallel texture operations indicated by the loaded array of state variables.

2. (previously amended) The method of claim 1, wherein the loading further comprises for each parallel texture pipeline:

receiving the array of state variables in an accumulator; and

transferring the received array of state variables to a latching register.

3. (previously amended) The method of claim 2, wherein the transferring is performed substantially simultaneously for each parallel texture pipeline, prior to the enabling.

4. (previously amended) The method of claim 1, further comprising disabling the processing portions of the remaining non-enabled parallel texture pipelines.

5. (previously amended) The method of claim 4, further comprising removing power to the disabled processing portions.

6. (currently amended) A method of synchronizing parallel texture pipelines, comprising:

accumulating in an accumulation portion of each parallel texture pipeline a set of state variable data for a polygon;

determining a number N of textures to be applied to the polygon, based on the set of state variable data; and

for each N parallel texture ~~pipeline~~ pipelines, simultaneously advancing the accumulated set of state variable data from the accumulation portion to a downstream processing portion.

7. (previously amended) The method of claim 6, further comprising disabling downstream processing portions of the remaining parallel texture pipelines.

8. (original) The method of claim 6, wherein the accumulating comprises:

receiving new state variable data, the new state variable data being defined differentially with respect to old state variable data previously accumulated, and

evicting obsolete elements of the old state variable data in favor of the new state variable data.

9. (currently amended) A control method for a texture processing system having multiple parallel texture pipelines, comprising:

in each parallel texture pipeline, accumulating state variable data for a polygon in an accumulation register, elements of the array of state variable data being received over a plurality of clock cycles; and

if the texture processing system switches texture modes, transitioning from a first number of active texture pipelines to a second number of active texture pipelines; and then substantially simultaneously, in each of the second number of active texture pipelines, advancing the array of state variable data from the accumulation register to a remainder processing portion.

10. (previously amended) The method of claim 9, further comprising:

enabling power to the second number of active texture pipelines; and

disabling power to the remaining texture pipelines.

11. (previously amended) A texture processing system, comprising:

a plurality of parallel texture pipelines, each parallel texture pipeline having a state variable queue, each state variable queue comprising an accumulation register for accumulating a set of state variables for a polygon, a latching register coupled to the accumulation register, and a state variable FIFO buffer coupled to the latching register; and

a controller having a data output coupled to the plurality of accumulation registers, the controller having a first control output to trigger the advance of the set of state variables from the plurality of accumulation registers to the plurality of latching registers, and the controller having a second control output to trigger the advance of the set of state variables from a number of the

latching registers to their corresponding state variable FIFO buffers, said number representing a number of parallel textures indicated by the set of state variables.

12. (previously amended) The texture processing system of claim 11, wherein said controller further comprises a data input to receive a state variable from a programming source.

13-17. (cancelled).

18. (previously submitted) A texture processor, comprising:

a first parallel texture pipeline having a first state variable queue including a first accumulator for receiving polygon state variables, a first latching register interoperably connected to the first accumulator, and a first texture processing FIFO interoperably connected to the first latching register;

a second parallel texture pipeline having a second state variable queue including a second accumulator for receiving the polygon state variables, a second latching register interoperably connected to the second accumulator, and a second texture processing FIFO interoperably connected to the second latching register;

a controller having an input for receiving a stream of data for a polygon including the polygon state variables, said controller having a first output for forwarding the polygon state variables to the first accumulator and the second accumulator, said controller having a second output for a state variable advance signal to trigger substantially simultaneously the transfer of the polygon state variables from the first accumulator to the first latching register and the transfer of the polygon state variables from the second accumulator to the second latching register, said controller having a third output for a first pipeline advance signal to transfer the polygon state variables from the first latching register to the first texture processing FIFO, and said controller having a fourth output for a second pipeline advance signal to transfer the polygon state variables from the second latching register to the second texture processing FIFO only when the polygon state variables indicate multiple parallel texture operations.

19. (previously submitted) A computer system, comprising:

a processor coupled to a bus;

a system memory in communication with the bus; and

a graphics unit comprising the texture processor of claim 18.

20. (previously submitted) A method for synchronizing parallel texture pipelines, comprising:

accumulating a set of state variables for a polygon in a first state variable accumulator of a first texture pipeline and in a second state variable accumulator of a second texture pipeline;

simultaneously transferring the set of state variables from the first state variable accumulator to a first state variable latching register of the first texture pipeline and from the second state variable accumulator to a second state variable latching register of the second texture pipeline;

advancing the set of state variables from the first state variable latching register to a remaining portion of the first texture pipeline; and

advancing the set of state variables from the second state variable latching register to a remaining portion of the second texture pipeline only when the set of state variables indicate two parallel texture operations for the polygon.